THAT WHICH IS CLAIMED IS:

1. A data path, comprising:

a downstream stage that strobes data at an input thereof responsive to a first control signal;

an upstream stage that sends data to the input of the downstream stage responsive to a second control signal; and

a control circuit operative to fix timing of the second control signal to timing of the first control signal.

2. A data path according to Claim 1, wherein the upstream stage comprises a first upstream stage, and wherein the data path further comprises a second upstream stage that sends data to an input of the first upstream stage responsive to a third control signal having a timing with respect to the second control signal that varies responsive to a frequency at which data is transferred along the data path.

3. A data path according to Claim 2, wherein a time interval between assertion of the third control signal and assertion of the second control signal decreases responsive to an increase in the frequency at which the data is transferred along the data path.

4. A data path according to Claim 2, wherein the control circuit comprises a fixed delay circuit that generates the first control signal from the second control signal.

5. A data path according to Claim 4, wherein the fixed delay circuit comprises a fixed delay circuit in a forward path of a delay locked loop (DLL) or a phase locked loop (PLL).

6. A data path according to Claim 2, wherein the control circuit is further operative to selectively fix timing of the second control signal to one of timing of the first control signal and timing of the third control signal.

7. A data path according to Claim 6, wherein the control circuit comprises a first fixed delay circuit operative to generate the first control signal from the second control signal and a second fixed delay circuit operative to generate the second control signal from the third control signal.

8. A data path according to Claim 6, wherein the control circuit is operative to allow relative timing of the third control signal with respect to the second control signal to vary with the frequency at which the data is transferred along the data path when timing of the second control signal is fixed to timing of the first control signal.

9. A data path according to Claim 2:

wherein the data path comprises a third upstream stage that sends data to the second upstream stage responsive to a fourth control signal; and

wherein the control circuit is further operative to fix timing of the fourth control circuit to timing of the third control signal.

10. A data path according to Claim 9, wherein the control circuit comprises a fixed delay circuit operative to generate the third control signal from the fourth control signal.

11. A data path according to Claim 9:

wherein the data path comprises a fourth upstream stage that sends data to an input of the third upstream stage responsive to a fifth control signal; and

wherein the control circuit is further operative to selectively fix timing of the fourth control signal to one of timing of the fourth control signal or timing of the fifth control signal.

12. A data path according to Claim 11, wherein the control circuit is further operative to fix timing of the second control signal to one of timing of the first control signal or timing of the third control signal.

13. A data path according to Claim 1, wherein the upstream stage comprises a level-enabled data receiver circuit.

14. A data path according to Claim 13, wherein the level-enabled data receiver circuit comprises a sense amplifier circuit.

15. A data path according to Claim 14, wherein the downstream stage comprises a flip-flop circuit.

16. An integrated circuit memory device, comprising:

a clocked output buffer that latches data responsive to a clock signal;

a sense amplifier that passes data at an input thereof to an input of the clocked output buffer responsive to an enable signal; and

a control circuit operative to fix timing of the enable signal to timing of the clock signal.

17. A device according to Claim 16, wherein the sense amplifier comprises a first sense amplifier, wherein the enable signal comprises a first enable signal, and further comprising a second sense amplifier that sends the data to an input of the first sense amplifier responsive to a second enable signal having a timing with respect to the first enable signal that varies responsive to a rate at which the data is transferred through the first and second sense amplifiers.

18. A device according to Claim 17, wherein the control circuit comprises a fixed delay circuit that generates the clock signal from the first enable signal.

19. A device according to Claim 18, wherein the fixed delay circuit comprises a fixed delay circuit in a forward path of a DLL circuit or a PLL circuit.

20. A device according to Claim 17, wherein the control circuit is further operative to selectively fix timing of the first enable signal to one of timing of the clock signal and timing of the second enable signal.

21. A device according to Claim 20, wherein the control circuit comprises a first fixed delay circuit operative to generate the clock signal from the first enable

signal and a second fixed delay circuit operative to generate the first enable signal from the second enable signal.

22. A device according to Claim 20, wherein the control circuit is operative to allow relative timing of the second enable signal with respect to the first enable signal to vary with the frequency at which the data is transferred through the first and second sense amplifiers when timing of the first enable signal is fixed to timing of the clock signal.

23. A device according to Claim 17, further comprising a third sense amplifier that sends data to the second sense amplifier responsive to a third enable signal, and wherein the control circuit is further operative to fix timing of the third enable signal to timing of the second enable signal.

24. A device according to Claim 23, wherein the control circuit comprises a fixed delay circuit operative to generate the second enable signal from the third enable signal.

25. A device according to Claim 23, further comprising a fourth sense amplifier that sends data to an input of the third sense amplifier responsive to a fourth enable signal; and

wherein the control circuit is further operative to selectively fix timing of the third enable signal to one of timing of the second enable signal or timing of the fourth enable signal.

26. A device according to Claim 25, wherein the control circuit is further operative to fix timing of the second control signal to one of timing of the first control signal or timing of the third control signal.

27. A device according to Claim 16, wherein the upstream stage comprises a level-enabled data receiver circuit.

28. A device according to Claim 27, wherein the level-enabled data receiver circuit comprises a sense amplifier circuit.

29. A device according to Claim 27, wherein the downstream stage comprises a flip-flop circuit.

30. A method of operating a data path, the method comprising:

strobing data at an input of a downstream stage of the data path responsive to a first control signal;

sending data to the input of the downstream stage responsive to a second control signal; and

fixing timing of the second control signal to timing of the first control signal.

31. A method according to Claim 30, the upstream stage comprises a first upstream stage, and further comprising sending data from a second upstream stage to an input of the first upstream stage responsive to a third control signal such that timing of the third control signal with respect to the second control signal varies responsive to a frequency at which data is transferred along the data path.

32. A method according to Claim 31, wherein the first and second upstream stages comprise respective first and second sense amplifiers.

33. A method according to Claim 32, wherein the downstream stage comprises a flip-flop.

34. A method according to Claim 31, wherein fixing timing of the second control signal to timing of the first control signal comprises fixing timing of the second control signal to timing of the first control signal while transferring data through the data path at rate greater than a predetermined threshold rate, and further comprising fixing timing of the second control signal to timing of the third control signal while transferring data through the data path a rate less than the predetermined threshold rate.

35. A method of characterizing a data path comprising a first driver-receiver pair including a first driver circuit and a first receiver circuit and a second driver-receiver pair comprising a second driver circuit and a second receiver circuit, the method comprising:

fixing timing of an enable signal for the first driver circuit to timing of an enable signal for the first receiver circuit and fixing timing of an enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit while increasing a rate at which data is passed through the data path to determine a minimum delay between the second driver circuit and the second driver circuit; and

fixing timing of the enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit and fixing timing of the enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit while increasing a rate at which data is passed through the data path to determine a minimum delay between the first driver circuit and the first receiver circuit.

36. A method according to Claim 35, wherein fixing timing of the enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit and fixing timing of the enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit while increasing a rate at which data is passed through the data path to determine a minimum delay between the first driver circuit and the first receiver circuit comprises fixing timing of the enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit, fixing timing of the enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit and fixing timing of the enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit while increasing a rate at which data is passed through the data path to determine the minimum delay between the first driver circuit and the first receiver circuit.

37. A method according to Claim 35:

wherein fixing timing of an enable signal for the first driver circuit to timing of an enable signal for the first receiver circuit comprises providing a fixed delay between the enable signal for the first driver circuit and the enable signal for the first receiver circuit;

wherein fixing timing of an enable signal for the second receiver circuit to timing of a data strobe signal for a stage downstream of the second receiver circuit

comprises providing a fixed delay between the enable signal fir the second receiver circuit and the data strobe signal for the downstream stage;

wherein fixing timing of the enable signal for the first receiver circuit to timing of an enable signal for the second driver circuit comprises providing a fixed delay between the enable signal for the first receiver circuit and the enable signal for the second driver circuit; and

wherein fixing timing of the enable signal for the second driver circuit to timing of the enable signal for the second receiver circuit comprises providing a fixed delay between the enable signal for the second driver circuit and the enable signal for the second receiver circuit.

38. A method according to Claim 35, wherein the first and second driver circuits and the first and second receiver circuits comprise respective sense amplifiers.

39. A method according to Claim 37, wherein the downstream stage comprises a flip-flop.